UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,118	11/18/2003	Katsumi Shibayama	046124-5179	2756

9629 7590 08/09/2005

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,118	SHIBAYAMA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *17-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed on May 23, 2005 has been entered and forwarded to the Examiner on June 02, 2005 .

Therefore claims 1-16 as recited in the amendment are currently pending in the Application.

Claims 17-25 were previously withdrawn from consideration.

Election/Restrictions

Claims 17-25 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected groups, there being no allowable generic or linking claim.

Election was made **without** traverse in the reply filed on May 23, 2005.

Information Disclosure Statement

No further IDS have been filed after the one dated August 20, 2004.

Claim Rejections - 35 USC Section 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior ad are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattson et al. (U.S. Patent No. 6,426,991, herein after Mattson) and in view of Chappo et al. (U.S. Patent No. 6,510,195, herein after Chappo)

With respect to claim 1Mattson describes a back illuminated photodiode array comprising ; a first conductive type semiconductor substrate having a light-incident surface (Mattson figure 7 #64, fig. 12 # 142 , abstract 4 th line from bottom).

Mattson describes an opposite surface but does not specifically mention a plurality of recessed portions located opposite said light incident surface.

However Chappo a patent from the same filed of endeavor describes in figures 2 to 4 # 52, 54 and 10, etc.#120 and col. 11 lines 4-8 describe an opposite surface with a plurality of recessed portions located opposite said light-incident surface to provide an electrical path from contacts on a back side of the photosensitive device through the substrate and the front and the back surfaces are aligned to each other .

Therefore it would have been obvious t o one of ordinary skill in the art at the time of the invention to include the an opposite surface with a plurality of recessed portions located opposite said light-incident surface instead of Mattson's opposite surface in Mattson's device. The motivation to make the afore mentioned substitution is to provide an electrical path from contacts on a back side of the photosensitive device through the substrate and the front and the back surfaces are aligned to each other. (Chappo 2 lines 51-67 and col. 3 lines 1-12).

The remaining limitations of claim 1 are :

a plurality of second conductive type semiconductor regions spatially detached at

each bottom of said recessed portions; (Chappo col. 11 lines 5-8) wherein said semiconductor regions individually constitute pn junctions together with said semiconductor substrate. (Mattson figure 3 , Chappo col. 8 line 50-55)

With respect to claim 2 Mattson describes a back illuminated photodiode array according to claim 1 , wherein said semiconductor substrate regions between a plurality of said recessed portions constitute a frame part which is thicker than said recessed portions. (Chappo figure 15 and col. 12 lines 27-34.).

With respect to claim 3 Mattson describes a back illuminated photodiode array according to claim 1 , wherein said semiconductor substrate is composed of a single semiconductor substrate. (Chappo Figure 2 A# 52, col. 6 lines6-8).

With respect to claim 4 Mattson describes a back illuminated photodiode array according to claim 1 , wherein said semiconductor substrate is provided with a first semiconductor substrate having said light-incident surface and a second semiconductor substrate bonded to said first semiconductor substrate and having side walls of said recessed portions. (Chappo col. 6 lines47-49, fig. 10 col. 1 lines 3-7).

With respect to claim 5 Mattson describes a back illuminated photodiode array according to claim 4, further comprising an etching stop layer existing between said first semiconductor substrate and said second semiconductor substrate and having resistance to a specific etching agent to be used for said second semiconductor substrate. (Mattson col. 5 lines 8-9, and Chappo col.6 lines 6-15, it is inherent for a stop layer to resistant the etching agent for second substrate in order for the stop layer to function as a stop layer) .

With respect to claim 6 Mattson describes a back illuminated photodiode array according to claim 4, further comprising an insulation layer existing between said first semiconductor substrate and said second semiconductor substrate. (Chappo col. 7 lines 23-31, Mattson col.5 lines 24-25).

With respect to claim 7 Mattson describes a back illuminated photodiode array according to claim 2, comprising a plurality of electrode pads formed on each top surface of said frame pad and individually and electrically connected to said semiconductor regions. (Mattson col. 1 lines 31 to 57, Chappo col. 6 lines 12 to 19, col. 7 lines 35-48 , figures 2 and 6).

With respect to claim 8 Mattson describes a back illuminated photodiode array according to claim 7, further comprising: an electric insulation layer formed on said frame pad; (Chappo col. 7 lines 23-31, Mattson col.5 lines 24-25) and a conductive member formed on said electric insulation layer and connecting electrically said semiconductor regions with said electrode pads. (Mattson col. 1 lines 31 to 57, Chappo col. 6 lines 12 to 19, col. 7 lines 35-48 , figures 2 and 6).

With respect to claim 9 Mattson describes a back illuminated photodiode array according to claim 8, wherein said electric insulation layer is provided with a contact hole for connecting an end of said conductive member to said semiconductor regions. (Chappo figure 10).

With respect to claim 10 Mattson describes a back illuminated photodiode array according to claim 2, where In said semiconductor regions extend from said bottoms to side surfaces of said recessed portions. (Chappo figure 10, col. 1 lines 5-7).

With respect to claim 11 Mattson describes a back illuminated photodiode array according to claim 2: wherein said semiconductor regions extend from said bottoms over side surfaces of said recessed portions to a top surface of said frame pad. (Chappo figure 9, col. 9 lines 60 -col. 10 line 20).

With respect to claim 12 Mattson describes a back illuminated photodiode array according to claim 11, comprising: an electric insulation layer formed on said frame pad and having a contact hole opposing said top surface; and electrode pads electrically connected to said semiconductor regions through said contact hole. (Chappo figure 10, col. 10 line 30- col. 1 1 line 7).

With respect to claim 13 Mattson describes a back illuminated photodiode array according to claim 2, wherein said frame part is provided with a first conductive type separation region higher in impurity concentration than said semiconductor substrate.(Chappo col. 12 line 47-49, as Chappo's semiconductor substrate described in col. 6 lines 6-8 is not doped and first conductive type separation region on frame is doped , the first conductive type separation region has higher impurity concentration than the substrate) .

With respect to claim 14 Mattson describes a back illuminated photodiode array according to claim I wherein an opening' size of said recessed portions decreases withan increase in the depth of said recessed portions.(well known in the art to decreasing recessed portion).

With respect to claim 15 Mattson describes a back illuminated photodiode array according to claim 1 , wherein said light-incident surface side of said semiconductor

substrate is provided with a first conductive type accumulation layer which is higher in impurity concentration than said semiconductor substrate. (Chappo col. 12 line 47-49, as Chappo's semiconductor substrate described in col. 6 lines 6-8 is not doped and first conductive type separation region on frame is doped , the first conductive type separation region has higher impurity concentration than the substrate and fig. 14 ,vias and conductive type accumulation layer on first surface and col.12 lines22-25).

B. Claim 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattson et al. (U.S. Patent No. 6,426,991 , herein after Mattson) and Chappo et al. (U.S. Patent No. 6,510,195, herein after Chappo) as applied to claims 1-13 and 15 above and further in view of Yamanaka et al. (U.S Patent No. 6,372,558, herein after Yamanaka).

With respect to claim 16 Mattson describes a back illuminated photodiode array according to claim 4, wherein mutually opposing surfaces of said first semiconductor substrate and said second semiconductor substrate are different in their crystal plane orientation.

Mattson and Chappo describe a back illuminated photodiode array according to claim 4 but do not specifically describe the first and the second semiconductor substrates to be in different in their crystal plane orientation.

However, Yamanaka in figure 8A and col. 13 line 60- col. 14 line 20 describes the first and the second semiconductor substrates to be in different in their crystal plane orientation to increase stability of the device increase productivity and enhance

mechanical and electronic properties of the surface .

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Yamanaka's the first and the second semiconductor substrates to be in different in their crystal plane orientation In Chappo's device to increase stability of the device increase productivity and enhance mechanical and electronic properties of the surface .

Response to Arguments

Applicant's arguments filed on June 02, 2005 have been fully considered but they are not persuasive for the following reasons :

Applicants' first contention that Mattson elements 42/64 are daughter board, ceramic substrate and do not describe a the first conductive type semiconductor substrate having a light-incident surface" features of independent claim 1, is not persuasive because as applicants' agree element 64 is ceramic substrate and as seen from figure 7 ceramic substrate 64 has photodiode 50 thereon .

It not understood how the photodiode 50 will function as a photodiode is light is not incident thereon and the ceramic substrate 64 on which the photodiode 50 is placed.

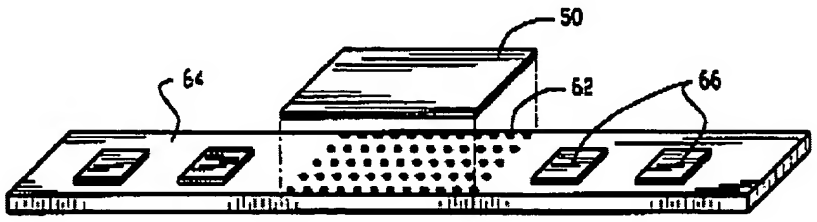


Fig. 7

Applicants' second contention that the last 4 lines of the abstract are not relevant is based on a improper understanding of the cited portion because the cited portion is

referred to as showing elements 42/64 to be substrates, which when further gleamed from figure 7 clearly shows substrates 42/64 to be substrate having a light-incident surface, it is further noted that by definition semiconductors are conducting.

Applicants' next contention that Chappo in figure 10, #120 and col. 11 lines 4-8 does not describe an opposite surface with a plurality of recessed portions located opposite said light-incident surface because element 120 is allegedly not a B-IP (back light photodiode array) assuming arguendo to be correct does not diminish the teachings of Chappo because as shown below in figures 2- 4 etc. a plurality of recessed portions next to bond pads 54 on B-I-P array 52 and located opposite said light incident surface (substrate 58) .

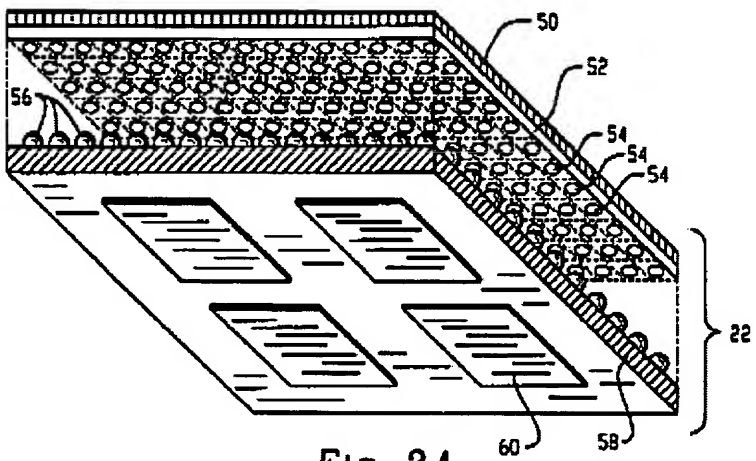
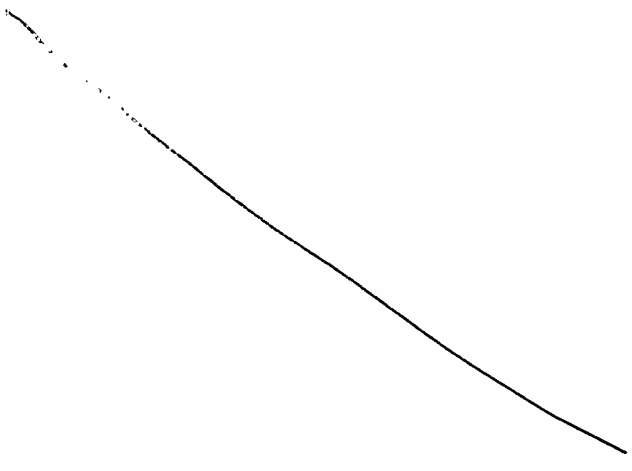


Fig. 2A

Therefore even assuming arguendo Applicants' argument is correct, still Chappo teaches/ describes an opposite surface with a plurality of recessed portions located opposite said light-incident surface.

Applicants' next contention that , " at the first paragraph of page 6, the Office Action asserts that the "remaining limitations of claim 1 are: a plurality of second conductive type semiconductor regions spatially detached at each bottom of said recessed portions; (Chappo col. 1 1 lines 5-8) wherein said semiconductor regions individually constitute pn junctions together with said semiconductor substrate. (Mattson figure 3, Chappo col. 8 line 50-55).', Applicants respectfully traverse these interpretations of Chappo because element 120 of Chappo is not a back-illuminated photodiode (BIP), but instead is an ASIC 258, as previously discussed " is not persuasive because Chappo additionally in figures 2,4 describes B-IP 52 and recessed portions next to bumps 54 as shown above.

Applicants next contention that Mattason/ Chappo do not describe in particular, the feature recited in independent claim 1 of providing spatially detached regions that constitute pn junctions in a manner that is neither shown nor suggested by Mattson is not persuasive because claim 1 merely recites,"a plurality of second conductive type semiconductor regions spatially detached at each bottom of said recessed portions; wherein said semiconductor regions individually constitute pn junctions together with said semiconductor substrate." And giving the broadest possible interpretation , Mattson figure shows :



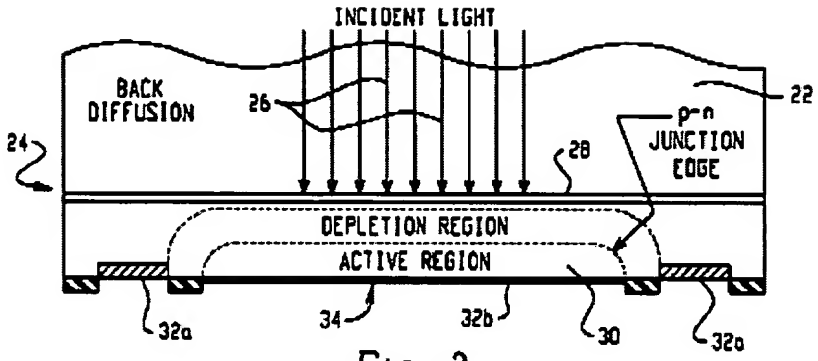


Fig. 3

It is inherent that a plurality of second conductive type semiconductor regions spatially detached at each bottom of said recessed portions because semiconductor layer having recessed portions will have the remaining portions spatially detached from each bottom of the recessed portions.

Further as shown in figure 3 , Mattson shows pn junctions .

Applicants' next contention that Chappo does not describe in figure 10, etc. #120 and col. 11 lines 4-8 an opposite surface with a plurality of recessed portions located opposite said light-incident surface to provide an electrical path from contacts on a back side of the photosensitive device through the substrate and the front and the back surfaces are aligned to each other", because element 120 in figure 10 of Chappo is not a photodiode is a photodiode or back light photodiode is a repeatition of the above argument that is not persuasive for reasons set out above i.e. is not persuasive because Chappo additionally in figures 2,4 describes B-IP 52 and recessed portions next to bumps 54 as shown above.

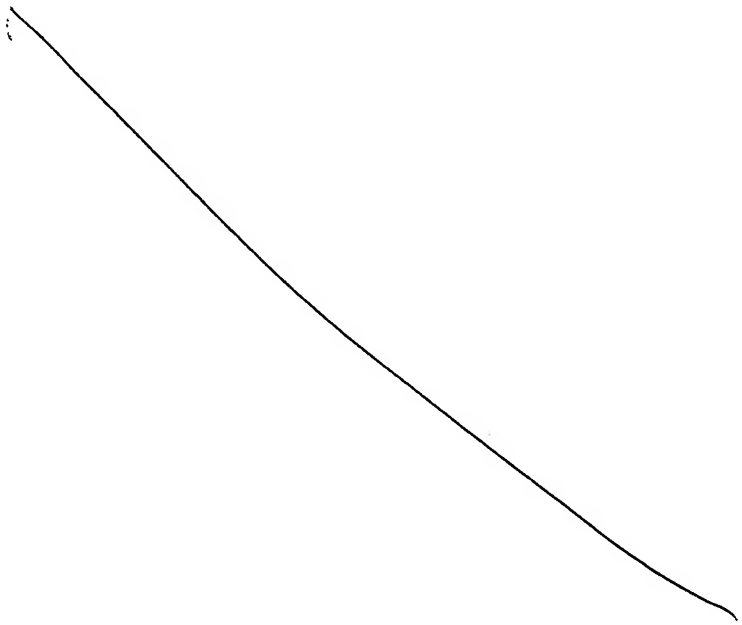
Therefore none of Applicants' arguments are persuasive and all the claims are finally rejected.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H Loo

LONG PHAM
PRIMARY EXAMINER